15.43/58

#13A Amdt Davis 3/11/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	)	Group Art Unit: 2823
NAMATAME et al.	)	
Serial No. 09/847,163	)	Examiner: Foong, Suk San
Filed: May 1, 2001	)	
For: SEMICONDUCTOR DEVICES AND METHODS FOR MANUFACTURING THE SAME	)	**AMENDMENT**

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sirs:

In response to the Office Action dated August 14, 2002, the response being due by Feb. 14, 2003 by the enclosed petition for extension of time, please enter and consider the following.

IN THE SPECIFICATION:

On page 1, please delete the first paragraph and insert the following in its place:

--Applicants hereby incorporate by reference Japanese Application No. 2000-132339, filed May 1, 2000 in its entirety. Applicants hereby incorporate by reference U.S. Application Serial No. 09/847,071, now U.S. Patent 6,580,088 in its entirety.--

3/29/04

IN THE CLAIMS:

Please amend claims 6, 9, 14 and 16 as follows:

6. (amended) A method for manufacturing a semiconductor device comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer, the method comprising: